AMENDMENTS TO THE DRAWINGS

Please Amend Figs. 13, 34, and 35 as provided in the replacement sheets accompanying this amendment.

REMARKS

This amendment is in response to the Official Action dated June 8, 2007. Claims 1, 10-25, 40-45, 54-58 have been amended; as such claims 1-3, 10-25, 40-45, 54-58 are now pending in this application. Claims 1, 10, 17, 40, and 54 are independent claims. Reconsideration and allowance is requested in view of the claim amendments and the following remarks.

No new matter has been added by this Amendment. Support for the amended claims can be found in the specification as filed. For example, support for the feature is described in connection with "*wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input to an effective pixel area*" is found in Figs. 2 and 3 and the corresponding description in the specification.

Applicant thanks the Examiner for the acknowledgement of priority under 35 U.S.C. § 119.

Applicant acknowledges and thanks the Examiner for the consideration of the references listed in the Information Disclosure Statement filed December 15, 2003.

Objections to the Drawings

Figs. 13, 34, and 35 have been amended to include the term "related art."

Page 6, line 24, has also been amended in the specification to replace a typographical error. The term "1B" has been replaced with the term "11B."

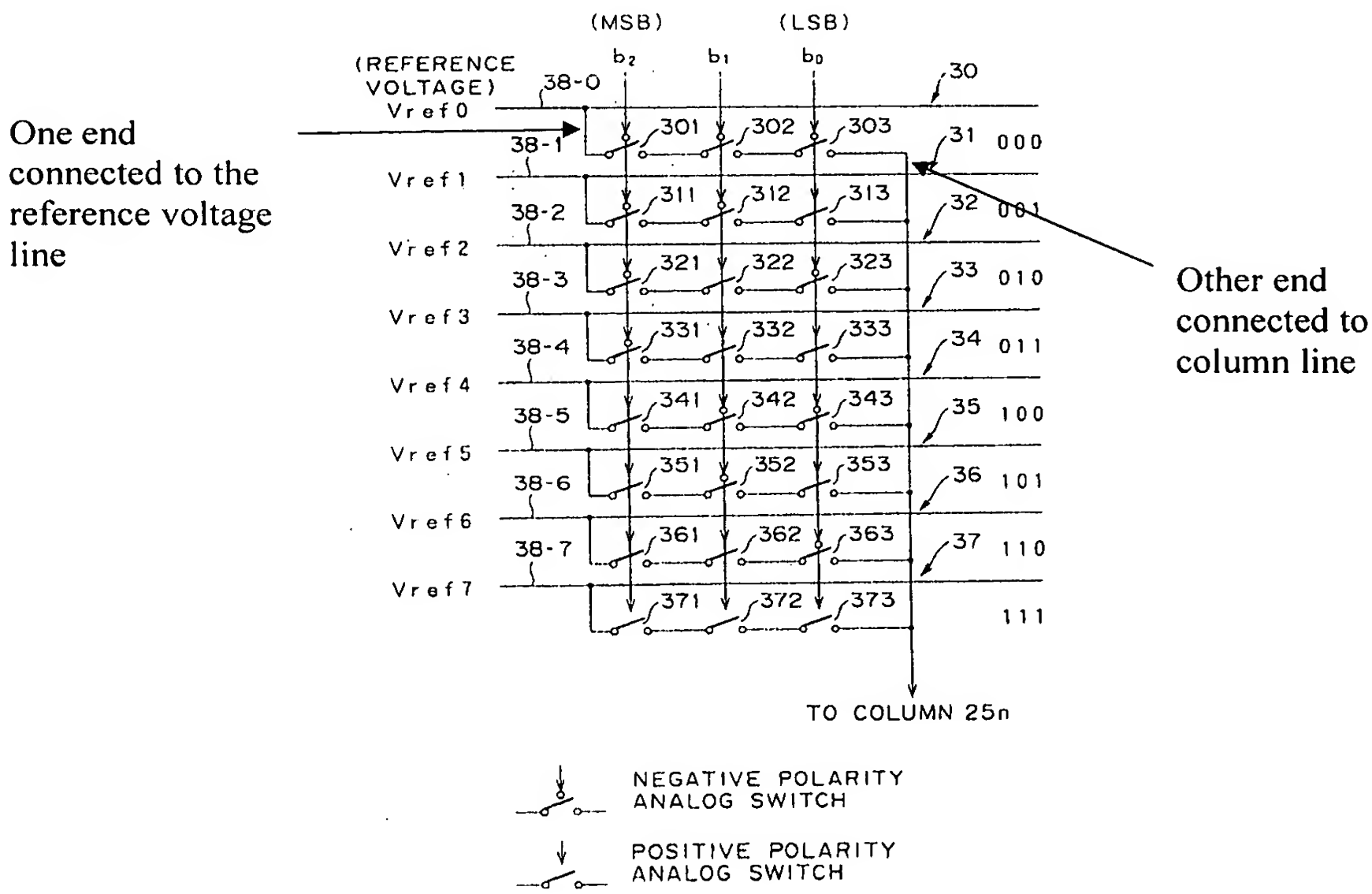
Accordingly, withdrawal of these objections is respectfully requested.

Objections to the Specification

The Abstract has been amended to conform to the standards set forth in the Office Action. Accordingly, withdrawal of this objection is respectfully requested.

Example Embodiment

Fig. 3 illustrates an example embodiment of the present invention. The example embodiment includes step-select units (301, 302, 303,...,373) connected at one end to a reference voltage line (38-0, 38-1,...,38-7) and at the other end to column line 25n.



(Fig 3 from Present Application, Emphassis added)

Rejections under 25 U.S.C. § 102

Claims 1-3 have been rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,911,926 to Koyoma et al. ("Koyoma"). Applicant respectfully traverses this rejection.

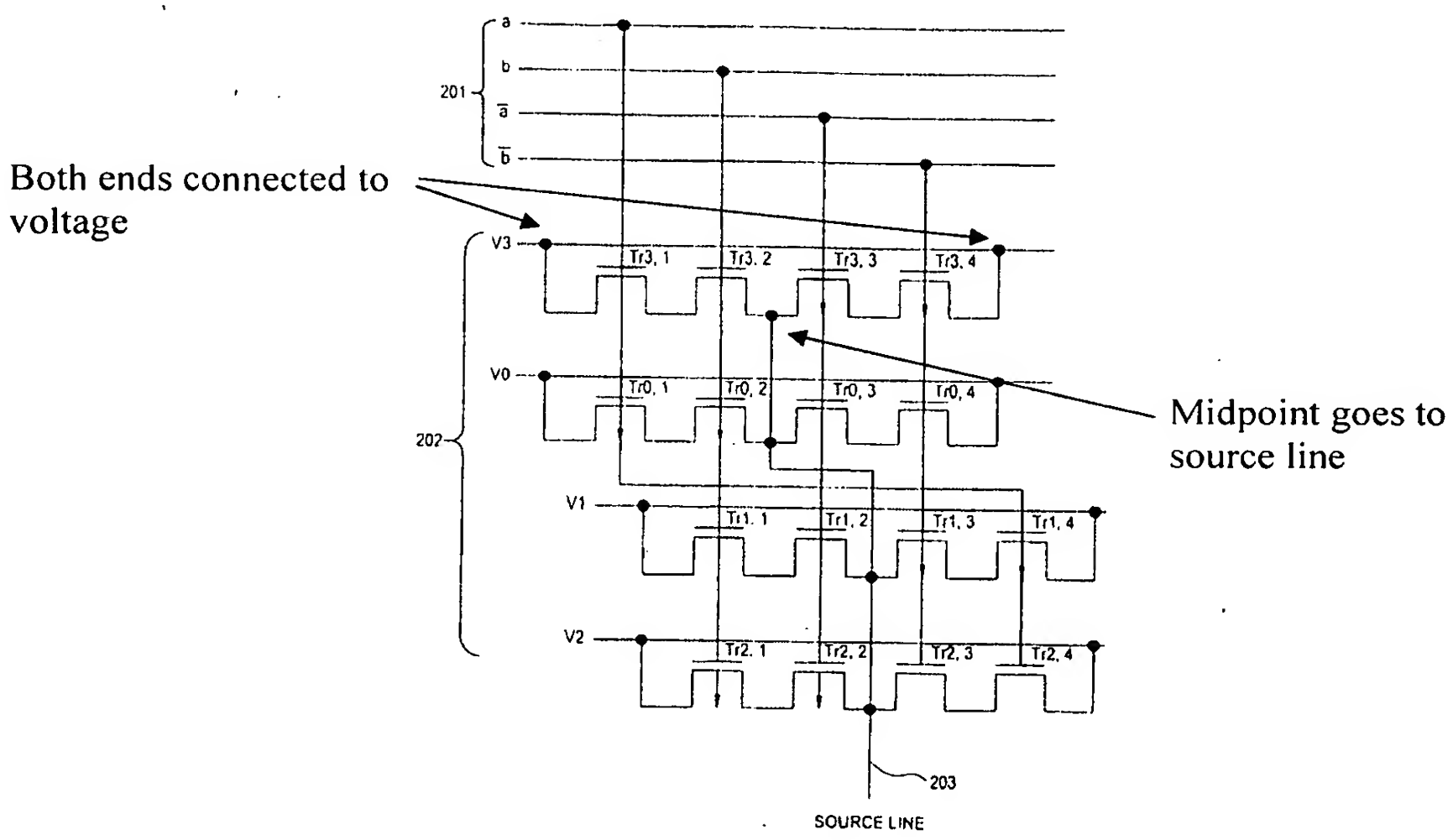
Amended claim 1 recites: *[a] digital-analog converter circuit for converting an n-bit (n is an integer of 2 or more) digital data signal comprising 2^n step select units connected*

across 2^n reference voltage lines, each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal;

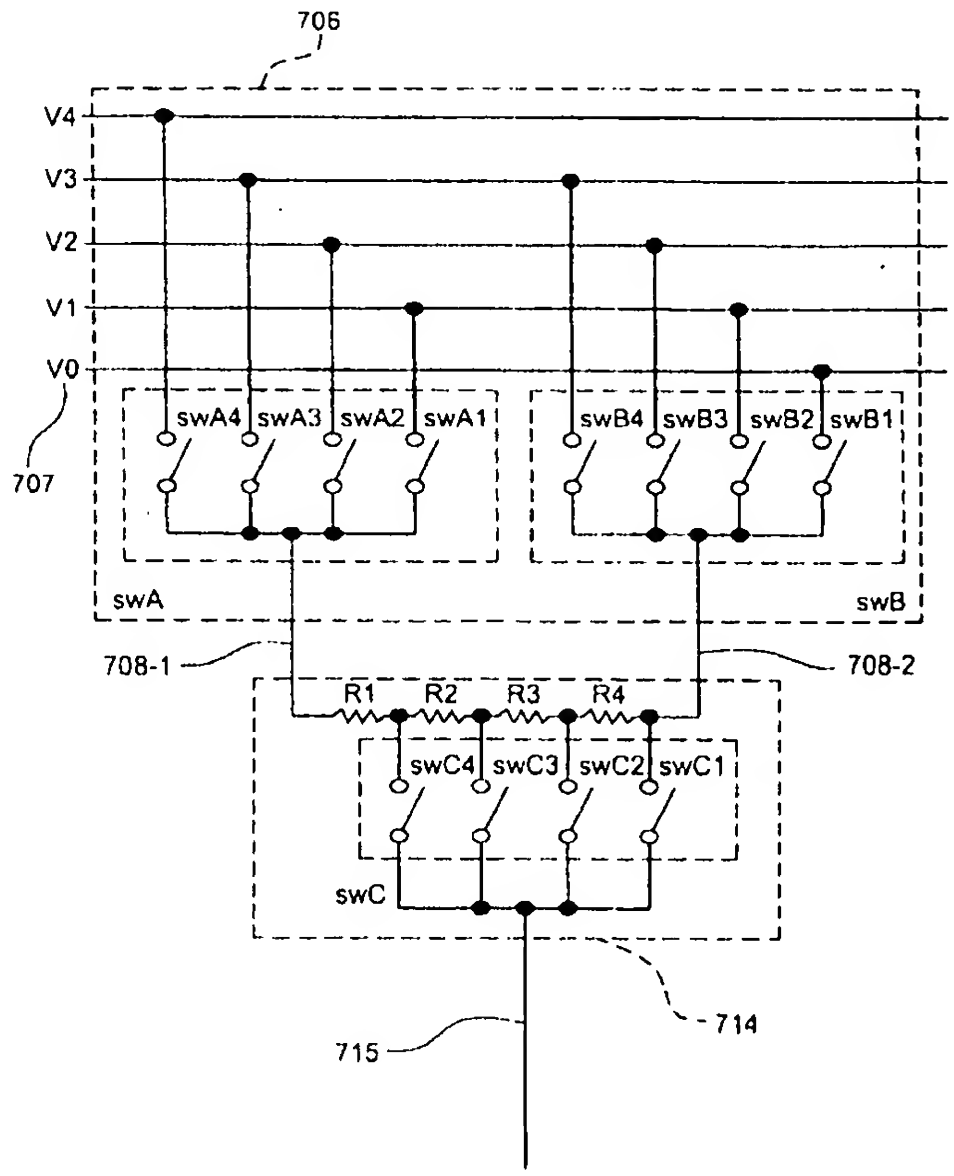
wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input of an effective pixel area.

With respect to claim 1, Koyoma fails to teach or suggest "*wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input of an effective pixel area.*"

Fig. 2 of Koyoma illustrates the transistor arrangement of a D/A conversion circuit. It is evident that both ends of the step select units comprising $Tr_{3,1}$, $Tr_{3,2}$, $Tr_{3,3}$, $Tr_{3,4}$, are connected to the same reference voltage line (V3), and it is the midpoint, not the "other end," of the step select unit that is connected to the source line.



The Office Action cites to page 4, asserting that Koyoma anticipates claim 1. Particularly, the office action compares the "*digital-analog converter circuit*" in claim 1 to the D/A converter disclosed in Koyoma. The Office Action cites to columns 25-26 of Koyoma, which describe Fig 9. Fig. 9 of Koyoma provides a schematic of a D/A conversion circuit. Like the circuit described above with reference to Fig. 3, the A/D Circuit in Fig. 9, also fails to teach or suggest "*[a] digital-analog converter circuit for converting an n-bit (n is an integer of 2 or more) digital data signal comprising 2^n step select units connected across 2^n reference voltage lines, each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal; wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line in effective pixel area.*"



(Fig. 9 of Koyoma)

First, Fig. 9 of Koyoma does not teach that "*each step select* ***unit including n serially connected analog switches*** *polarized to match a logic state of each bit of the n-bit digital data signal.*" As is evident, the switches are all connected in parallel to their respective reference voltages. Second, claim 1 recites that each step unit is connected to "*the reference voltage*", i.e., there is one reference voltage to which each step unit is connected. However, in Koyoma, each switch is connected to its own reference voltage, such that the step select circuits in Fig. 9 are connected to a plurality of voltages. Finally, even if Fig. 9 did disclose that the switches were in serial, which clearly they are not, Fig. 9 still fails to teach that one end of the step select units are all connected to the reference voltage lines and it is the midpoint of the step select unit, not the "other end," of the step select unit that would be connected to the source line.

Koyoma therefore fails to teach or suggest various features of independent claim 1. Furthermore, at least for the reason disclosed above claims 2-3, overcome Koyoma because they depend on independent claim 1.

Claims 1-3 have been rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,274,869 to Butler et al. ("Butler"). Applicant respectfully traverses this rejection.

Amended claim 10 recites: *[a] liquid crystal display comprising:*

a digital-analog converter circuit for converting an n-bit (n is an integer of 2 or more) digital data signal comprising 2^n step select units connected across 2^n reference voltage lines, each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal;

wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input to an effective pixel area;

and a level shift circuit for converting a low voltage amplitude signal to a high voltage amplitude signal comprising:

a CMOS latch cell having two input sections,

wherein a first resistor element is inserted between each of the two input sections and two signal sources.

With respect to claim 10, Butler fails to teach or suggest, at least, "*a digital-analog converter circuit for converting an n-bit (n is an integer of 2 or more) digital data signal comprising 2n step select units connected across 2n reference voltage lines, each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal; wherein one end of each of said step select units is connected to the reference voltage line and the other end of each of said step select units is connected to a column line input to an effective pixel area.*"

Butler is directed to an offset correction circuit for a focal point array. The offset correction circuit serves to correct for non-uniformity among sensor element output. This ensures that when a plurality of sensors are used in an array, the output of various sensors can be normalized.

Butler does not disclose a "*digital-analog converter circuit for converting an n-bit (n is an integer of 2 or more) digital data signal comprising 2n step select units connected across 2n reference voltage lines.*"

Butler therefore fails to teach or suggest various features of independent claim 10. For similar reasons, Butler fails to teach or suggest various features of claims 17, 40, and 54. Furthermore, at least for the reason disclosed above claims 11-16, 18-25, 41-45, and 55-58 also overcome Butler because they depend on independents claims 10, 17, 40, and 54, respectively.

Accordingly, Applicant respectfully requests that the rejection of independent claim 1-3, 10-25, 40-45, and 54-58 under 35 U.S.C. § 102(e) be withdrawn.

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 18-0013, under Order No. SON-1697/DIV from which the undersigned is authorized to draw.

Dated: October 30, 2007

Respectfully submitted,

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